Register for Certification exam

Thank you for taking the Week 2 : Assignment 2.

Week 2 : Assignment 2

Your last recorded submission was on 2021-08-15, 12:18 IST

Due date: 2021-08-18, 23:59 IST.

1) Which of the following statement(s) is/are true for **radix** of a positional number system. *1 point*

a. It represents number of unique digits, used to represent numbers.
b. It represents number of binary digits, used to represent single digit of any number system.
c. Radix of Hexadecimal number system is 4.
d. Radix of Hexadecimal number system is 16.

- [x] a.
- [ ] b.
- [ ] c.
- [x] d.

2) What will be binary representation of $(3.6E)_{16}$? *1 point*

a. 0011 . 0110 1111
b. 0011 . 0110 1110
c. 11 . 0110 111
d. None of these

- [ ] a.
- [x] b.
- [x] c.
- [ ] d.

3) What is the largest number that can be represented using 10-bit 2's complement representation ------?

511

1 point

4) Consider the following statement for representing signed numbers using sign magnitude, 1's complement and 2's complement format:
(i) Sign of the number can be identified using MSB.
(ii) By flipping the sign bit we can obtain the number of its opposite sign.
Which of the following is correct?

1 point

a. Only (i) is true
b. Only (ii) is true
c. Both (i) and (ii) are true
d. Both (i) and (ii) are false

- (●) a.
- ( ) b.
- ( ) c.
- ( ) d.

5) Which of the following addressing modes does not require any memory access for fetching the operands?

1 point

a. Direct Addressing
b. Immediate Addressing
c. Register Indirect
d. Register Addressing
e. None of these

- [ ] a.
- [x] b.
- [ ] c.
- [x] d.
- [ ] e.

6) How do you represent -10 using 16-bit, 2's complement representation? *1 point*

a. 1000 0000 0001 0110
b. 0000 0000 0000 1010
c. 1111 1111 1111 0110
d. 0000 0000 0001 0110

- ○ a.
- ○ b.
- ◉ c.
- ○ d.

7) For the instruction **`STORE R1,35(R2)`** what will be effective address of the memory operand if R2 is 200 (in decimal)? *1 point*

a. 35
b. 165
c. 200
d. None of these

- ○ a.
- ○ b.
- ○ c.
- ◉ d.

8) Which of the following statement(s) is/are true for CISC architecture? *1 point*

a. Supports large number of addressing modes.
b. It does not support variable-length instruction.
c. Pipeline implementation of CISC architecture is complex.
d. Only load and store instruction can access memory

- ☑ a.
- ☐ b.
- ☑ c.
- ☐ d.

9) Which of the following instruction is/are invalid for MIPS32 processor if $s0 and $s1 contains address of some variables (say A and B). *1 point*

a. add $t0, $t1, 20($s0)
b. lw $t0, 40($s0)
c. add $t0, $t0, $t1
d. None of these

- ○ a.
- ○ b.
- ○ c.
- ◉ d.

10) Consider the following MIPS instruction: *1 point*

```
slt $t0, $s0, $s1
```

What does the instruction do if $s0 and $s1 is loaded with some data?

a. Set $t0 = 1 if $s0<$s1
b. Set $t0 = 0 if $s0>$s1
c. Set $t0 = 1 if $s0>$s1
d. Set $t0 = 0 if $s0<$s1

- ☑ a.
- ☑ b.
- ☐ c.
- ☐ d.

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers